ABSTRACT OF THE DISCLOSURE

Disclosed herein is a semiconductor memory device having a memory array comprising CMOS flip-flop circuit type memory cells, which is capable of improving a noise margin, making a read rate fast and reducing power consumption. In the semiconductor memory device, an operating voltage of the memory cell is set higher than an operating voltage of each of peripheral circuits. Threshold voltages of MOS transistors that constitute the memory cell, are set higher than those of MOS transistors constituting the peripheral circuit. A gate insulting film for the MOS transistors that constitute the memory cell, is formed so as to be regarded as thicker than a gate insulting film for the MOS transistors constituting the peripheral circuit when converted to an insulating film of the same material. Further, a word-line selection level and a bit-line precharge level are set identical to the level of the operating voltage of the peripheral circuit.